## ABSTRACT OF THE DISCLOSURE

The present invention provides a digital PLL device operating stably toward input of a signal having a broad frequency band, variations in environments and variations with time, and having the precision of the PLL which does not deteriorate even at a low operational frequency. The average of the maximum value and the minimum value of a digital signal in a predetermined period is used as a threshold. Rise times and fall times as times when the threshold and an approximated line of two values of the digital signal crosses are detected. The time intervals between the adjacent rise and fall times are obtained during a predetermined period. The minimum value of the time intervals is used as the input rate. The synchronous clock is output on the basis of the input rate and the rise and fall times. The synchronous clock as the clock input and the comparison signal which is obtained by comparing the threshold and the digital signal as the D input are supplied to the latch circuit, and then the synchronous signal is output.